Electronic Version
Stylesheet Version v1.1.1

[CYCLIC REDUNDANCY CHECK GENERATION CIRCUIT]

Abstract

A circuit, a method, and a method of designing the circuit, the circuit including: multiple W-bit packet data slice latches; a data partition comprising multiple data XOR subtree levels and having data latches between the data XOR subtree levels; a remainder partition comprising multiple remainder XOR subtree levels and having remainder latches between the remainder XOR subtree levels; a combinatorial XOR tree, outputs of the remainder partition and outputs of the data partition connected to inputs of the combinatorial XOR tree; and a remainder latch, combinatorial XOR tree connected to the remainder latch and the outputs of the remainder latch connected to the remainder partition.